



Quantum Circuit Simulation Using QuIDDs

Motivation

- Need for a better way to simulate quantum circuits

- Quantum Information Decision Diagram (QuIDD)
- Novel data representation that uses Binary Decision Diagrams (BDD) widely used in computer-aided circuit design
- Captures some exponentially-sized matrices and vectors in a form
- that grows polynomially with the number of qubits
- Multiplies matrices and vectors in compressed form
- QuIDDPro Simulator
 - Our QuIDD-based simulator implemented in C++
 Experiments with Grover's algorithm demonstrate fast execution and low memory utilization









MAT 14.0	B++ 0.22	QP 0.20	n	Oct	MAT	R++	on
14.0	0.22	0.20					OP .
45.0		0.20	10	3.60e-2	2.00e-2	1.95e-2	0.211
43.9	0.72	0.39	11	6.80e-2	4.40e-2	7.03e-2	0.207
1.53e2	2.22	0.88	12	0.132	9.20e-2	7.42e-2	0.281
5.80e2	6.92	1.94	13	0.260	0.188	0.129	0.426
5.90e3	23.09	4.79	14	0.268	0.264	0.250	0,444
5.92e4	70.4	9.32	15	0.524	0.520	0.500	0.605
TIME-OUT	2.13e2	22.2	16	1.04	1.03	1.00	0.840
TIME-OUT	6.34e2	50.7	17	2.06	2.06	2.00	0.965
TIME-OUT	1.92e3	1.13e2	18	4.11	4.10	4.00	1.59
TIME-OUT	5.74e3	2.00e2	19	8.20	8.20	8.00	1.77
TIME OUT	174e4	3 25.02	20	16.4	16.4	16.0	2.04
	5.80e2 5.90e3 5.92e4 TIME-OUT TIME-OUT TIME-OUT TIME-OUT	5.80e2 6.92 5.90e3 23.09 5.92e4 70.4 TIME-OUT 2.13e2 TIME-OUT 6.34e2 TIME-OUT 1.92e3 TIME-OUT 5.74e3	5.80c2 6.92 1.94 5.90c3 23.09 4.79 5.92c4 70.4 9.32 TIME-OUT 2.13c2 22.2 TIME-OUT 6.34c2 50.7 TIME-OUT 1.3c2 1.3c2 TIME-OUT 1.92c3 1.13c2 TIME-OUT 5.74c3 2.00c2	5.80c2 6.92 1.94 13 5.90c3 23.09 4.79 14 5.92c4 70.4 9.32 15 TIME-OUT 2.13c2 22.2 16 TIME-OUT 6.34c2 50.7 17 TIME-OUT 1.92c3 1.3c2 18 TIME-OUT 1.92c4 3.12c1 18	5.80c2 6.92 1.94 13 0.260 5.90c3 23.09 4.79 14 0.268 5.92c4 70.4 9.32 15 0.524 TIME-OUT 2.13c2 22.2 16 1.04 TIME-OUT 6.34c2 50.7 17 2.06 TIME-OUT 1.92c1 1.3c2 18 4.11 TIME-OUT 5.74c3 2.00c2 19 8.20	5.80c2 6.92 1.94 13 0.260 0.188 5.90c3 23.09 4.79 14 0.268 0.264 5.92c4 70.4 9.32 15 0.524 0.524 TIME-OUT 2.13c2 22.2 16 1.04 1.03 TIME-OUT 1.92c3 1.13c2 17 2.06 2.06 TIME-OUT 1.92c3 1.02c 11 4.10 1.01 TIME-OUT 5.74c3 2.00c2 19 8.20 8.20	5.80c2 6.92 1.94 13 0.260 0.188 0.129 5.90c3 23.09 4.79 14 0.260 0.188 0.129 5.90c4 70.4 9.32 15 0.524 0.250 5.000 TIME-OUT 2.13c2 22.2 16 1.04 1.03 1.00 TIME-OUT 1.92c3 1.13c2 18 4.11 4.10 4.00 TIME-OUT 1.92c3 1.3c2 18 4.11 4.10 4.00 TIME-OUT 5.74c3 2.00c2 19 8.20 8.20 8.00







Quantum Circuit Synthesis

- · Synthesis of classical circuits
 - Given a truth table, it is easy to find a circuit
 - Gate-count minimization is trickier, but doable by hand for circuits with several inputs
- Synthesis of *n*-input quantum circuits
 - Given a $2^n x 2^n$ matrix, can find a circuit (known algorithm)
 - Gate-count minimization doable by hand only for one input
 - For two inputs, optimal constructions are less than one year old, involve taking square roots of 4x4 matrices...

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Two-qubit Computation with Minimum Resources

- 1. Some elementary gates have 2 inputs; our work allows to compare gate libraries
- 2. Most physical implementations of q. computers are currently restricted to 2 qubits
- 3. Circuits for quantum communication often have 2-3 inputs
- Given a qantum circuit with >2 inputs, we can look for <u>2-input subcircuits</u> and re-optimize those (peephole optimization)

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Only notaties	CNOT O	ver and U Sverall 1	CNOT 1	unds Overall	Circuit identities	Descriptions
$\{CHOT, R_y, R_z\}$ $\{CHOT, R_y, R_z\}$ $\{CHOT, R_z, R_z\}$	3	18 18 18	33	18 18 19	$C_{j}C_{j} = 1$ $\chi^{j,k}\chi^{j,k} = 1$ $C_{j}^{k}C_{j}^{k} = \chi^{j,k}C_{j}^{k}$	CNOT-gate cancellation SWAP-gate cancellation CNOT-pair elimination
Table 1. Constru counts for gene libraries. Each t	uctive upp ric circuits	per bou s using	ands or severation	10 10 I gate I gate	$ \begin{array}{c} C_{k}^{j}R_{k}^{j}(\theta)=R_{k}^{j}(\theta)C_{k}^{j},C_{k}^{j}S_{c}^{j}=S_{c}^{k}C_{k}^{j}\\ C_{k}^{j}R_{c}^{k}(\theta)=R_{c}^{k}(\theta)C_{k}^{j},C_{k}^{j}S_{c}^{j}=S_{c}^{k}C_{k}^{j}\\ C_{k}^{j}\chi^{j,k}=\chi^{j,k}C_{k}^{j}\\ V^{j}\chi^{j,k}=\chi^{j,k}V^{k} \end{array} $	move R_x , S_x via CNOT \oplus move R_z , S_z via CNOT • move CNOT via SWAP move 1-bit gate via SWAP
(CNOT) gates is tive overall bout	compatib	bound	the re	spec-	$R_n(\Theta)R_n(\phi) = R_n(\Theta + \phi)$ $\vec{n} \perp \vec{m} \implies S_nR_m(\Theta) = R_{n \times m}(\Theta)S_n$	merging R_n gates changing axis of rotation
In particular, we rotation gates. be tightened are	never use Bounds t shown in	e input that ma n bold.	-indepe ay pote	ndent ntially	Table 2. Circuit identities (used in our work.

Recent Work
 V. V. Shende, I. L. Markov and S. S. Bullock, ``On Universal Gate Libraries and Generic Minimal Two-qubit Circuits," <u>quant-ph/0308033</u> V. V. Shende, S. S. Bullock and I. L. Markov, ``Recognizing Small-Circuit Structure in Two- Qubit Operators," <u>quant-ph/0308045</u>
George F. Viamontes, Igor L. Markov and John P. Hayes, ``Improving Gate-Level Simulation of Quantum Circuits," <u>quant-ph/0309060</u>