To qzhwang@glove.cs.uic.edu, djariwal@glove.cs.uic.edu, cnchu@iastate.edu, nataraj@iastate.edu, panmin@eng.iastate.edu, royj@eecs.umich.edu, imarkov@eecs.umich.edu, xie@CS.UCLA.EDU, cong@CS.UCLA.EDU, pmadden@acm.org, pmadden@cs.binghamton.edu, qiwang@cs.ucsd.edu, abk@cs.ucsd.edu, sreda@cs.ucsd.edu, f92921104@ntu.edu.tw, mms@ece.ucsb.edu, hb@ece.ucsb.edu, rutenbar@ece.cmu.edu, zxiu@ece.cmu.edu, frank.johannes@tum.de, obermeier@tum.de, stcauley@purdue.edu, g936342@oz.nthu.edu.tw, ylin@cs.nthu.edu.tw

cc Chuck Alpert/Austin/IBM@IBMUS, Gi-Joon Nam/Austin/IBM@IBMUS

bcc

Subject ISPD 2005 Placement contest: Important Notice

Hi Folks,

Hope everythig goes well with the released sample benchmarks. If you somehow didn't get those two benchmarks from me (adaptec1 & adaptec3), please let me know as soon as possible.

So far we have 13 teams that are willing to compete in this contest, and I think this is a good sign for a successful contest. However, the steering committee and I did not anticipate quite so many entries. While some of the contestants are entering placers that have evolved over years, others are just now developing their placers. The steering committee does not want to use up the time of the ISPD audience (and space in the ISPD proceedings) on a placer that is just being developed and may not work at all. The intent of the three page papers is to serve as somewhat of a placement tutorial of the current state of the art in academic placers. This should not be a forum to present some new placer that may not be up to the standards of existing technology.

Thus, we have decided to add an additional requirement that must be met in order to participate in the contest. You must submit your placement results on sample benchmarks (adaptec1 & adaptec3) and your placer binary to me by **Feb. 6th, Sunday**. Along with your binary, please supply a script that allows me to invoke it with one command; the placer should duplicate the results that you send me. The purpose of this new requirement is two-fold:

1) screening process: if your placer cannot generate at least reasonable placement results on these two sample circuits, it's very unlikely that your placer will work on contest benchmarks, because adaptec1 & adaptec3 are on the small side of the designs that will be used for contest.

2) simulation of contest process: I'd like to go through contest process in advance. In this way, there would be no unexpected problems during the real contest.

If you have any concerns, please let me know as soon as possible.

Here are the important dates to remember:
Jan. 28 : 3-page technical paper draft
Feb. 6: submission of placement results on sample benchmarks and binary
March 20th 5:00 pm to March 25th 5:00 pm: contest

Thanks and good luck.

Gi-Joon