OL_MPEG4
Single and Multi-Channel MPEG-4 Encoder

Rev 1.1

General Description

The OL_MPEG4 core family includes hardware implementations of single and multi-channel implementations of the MPEG-4 algorithm. The core accepts a full resolution video stream as input and outputs encoded bitstreams.
Simple, fully synchronous design with low gate count.

Applications

- Digital video recorders.
- Video wireless devices.
- Video surveillance systems.
- Hand held video cameras.

Features

- Full resolution video (beyond 4CIF (704x576) @ 30 fps) support.
- Very low operational frequency : from ~3 MHz for QCIF @ 15 fps.
- Multi-channel version proven in silicon. Single channel version proven in FPGA.
- Motion vector up to –16.0/+15.5 pixels with single and bi-directional search (I, P & B pictures).
- Glueless interface to SDRAM for frame storage (a single 16 Mbit or 64 Mbit SDRAM chip with 16 bit data bus is sufficient for most applications).
- The processor includes IEEE-1180 compliant DCT/IDCT and quantizer/dequantizer.
- Supports YCbCr 4:2:0 raster video input
- The core outputs MPEG-4 bitstreams.
- Min Clock speed = 8 x the raw pixel clock speed
- Simple, fully synchronous design.
- Available as fully functional and synthesizable VHDL or Verilog soft-core.

Functional Description

Motion estimation and compensation is at the heart of all standard video compression algorithms. This technique is used to exploit the temporal redundancy present in natural video sequences. All the pictures processed by the core are assumed to be divided into macroblocks (normally a block of 16x16 pixels).

Rather than exploiting spatial redundancy only (as in JPEG), temporal redundancy is exploited by transmitting the difference between a macroblock in the current picture and the best matching macroblock in a reference picture.

The block diagram of the internal Motion Processor is shown in the diagram below.

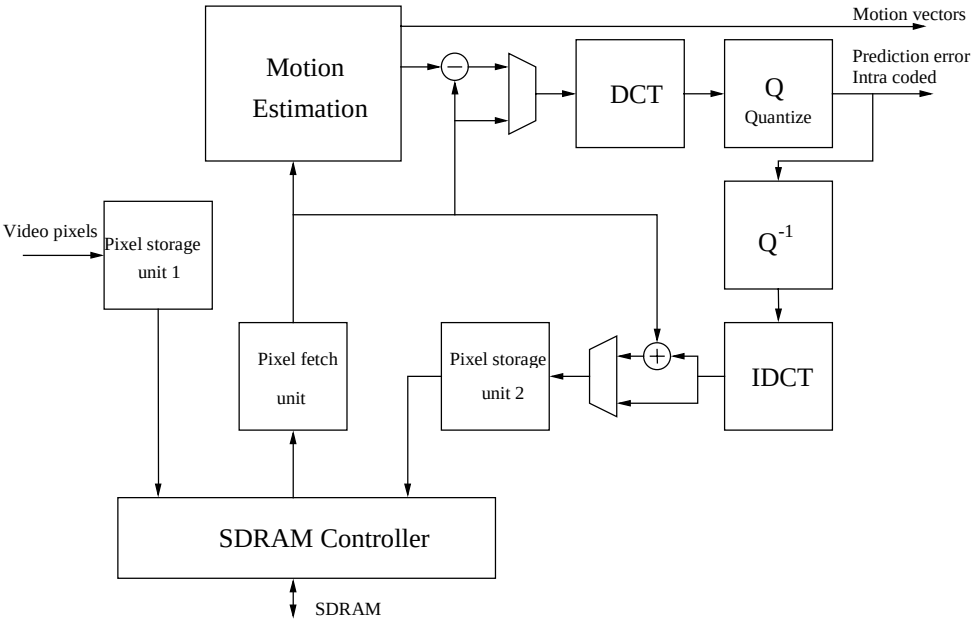

Figure 1 Motion Processor block diagram

The Motion Processor acts as a front end in the video compression algorithm. It accepts video YUV 4:2:0 in raster form and it outputs motion vectors as well as transformed, quantized error blocks.

This pre-processed data is then encoded by a MPEG-4 bitstream encoding stage shown in the figure below.

The Prediction unit receives the DC components of the intra macroblocks as well as the motion vectors from the OL_Motion core. This information is processed and passed to the Encoder unit to be merged with the transformed data being encoded. The Encoder unit can process intra and non intra macroblocks in I and P frames. Macroblock data is broken into (Intra,Level,Run,Last) codes that are individually encoded.

The bits packets produced by the Encoder unit are assembled by the Bit Packing unit before being output.
The core outputs I_VOP and P-VOP MPEG-4 Video Object Planes.

Other headers can be added with external devices. Only a few extra bytes of header data are required to produce a valid MPEG-4 Video Object Layer.

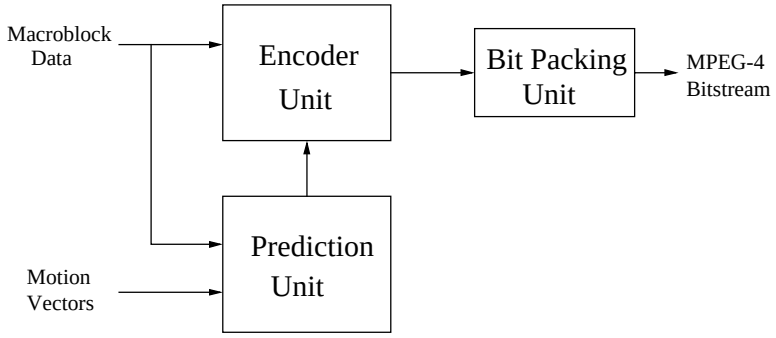

Figure 2 Bitstream encoder block diagram.

The diagram below shows the Motion Processor front end together with an MPEG-4 bitstream encoding back end. The diagram also shows a user provided CPU to set internal registers.

The CPU is not required by the encoding process as the registers can be set by other means.

A single 16 or 64 Mbit SDRAM chip with 16-bit wide data bus is sufficient as frame buffer.

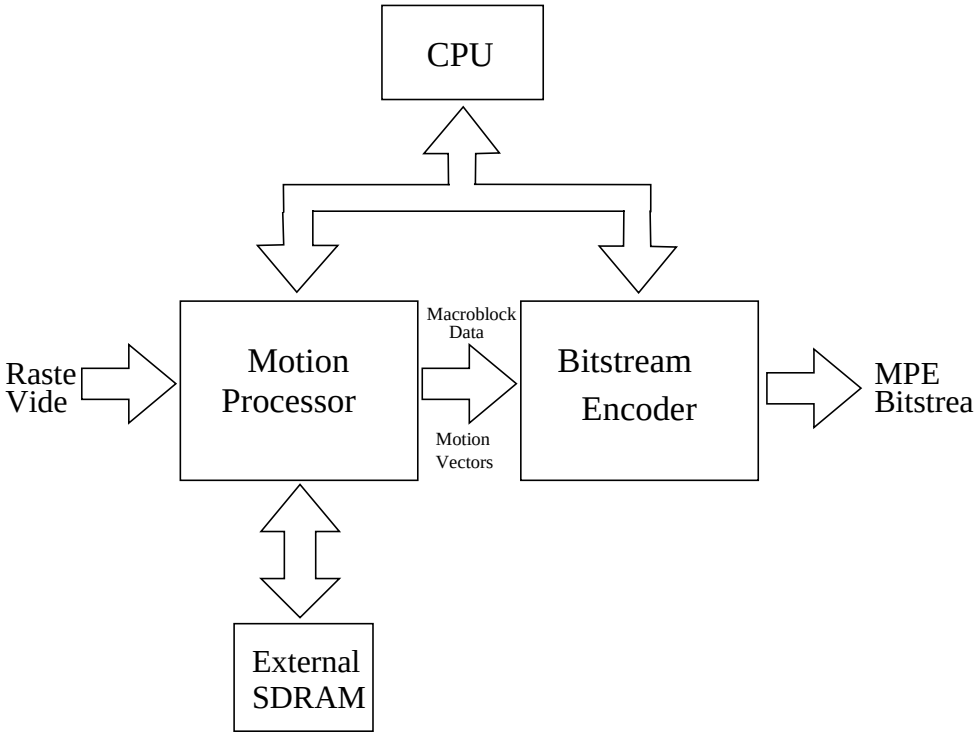

Figure 3 Internal structure of the OL_MPEG core.

The OL_MPEG4 core supports real time encoding of video up to full resolution at 30 fps.

The core is clocked at 8 times the raw pixel rate (for a video resolution of 640x480 at 30 fps, such frequency will be 640x480x30x8 = ~ 73.7 MHz).

The table below summarizes the relation between some common video resolutions and frame rates and the clock frequency of the cores.

Resolution	QCIF @ 15 fps	QCIF @ 30 fps	CIF @ 30fps	VGA @ 30 fps	4CIF @ 30 fps
Core freq.	~3 MHz	~6.1 MHz	~24.3 MHz	~73.7 MHz	~97.3 MHz

Table 1 Core frequency versus video resolution and frame rate.

This core is available in two different flavours : single and multi-channel.

The multi-channel version is essentially identical to the single channel version but it also contains some extra logic allowing to process up to 16 video channels of different resolutions and frame rates in a time multiplexing fashion.

The multi-channel version of the core has been proven in silicon in a video surveillance application.

Performance

Performance figures of the OL_MPEG4 core implemented with some particular technologies are shown in the table below.

Technology	Approx Area	Speed	Video Throughput
ASIC 0.18 u	39 Kgates + 25 Kbits RAM	~ 100 MHz	704x576 (4CIF) @ 30 fps
Virtex II	~3600 slices + 10 Multipliers + 16 RAM blocks	>70 MHz	640x480 @ 28fps

Table 2 Performance of the single channel OL_MPEG4 core.

Summary

The combination of low gate count, low operating frequency and full video resolution support makes of this core family an application-enabling technology.

The applications of this core range from low power wireless application at relatively low resolution to full resolution handheld and video surveillance cameras.

The very small area of this core also allows novel applications such as its direct integration on a CMOS sensor. This would create an extremely compact intelligent sensor accepting light directly at its input and outputting an MPEG bitstream directly.

Deliverables

Synthesizable VHDL or Verilog RTL.
Bit accurate C model.
Complete HDL testbench.
Complete data sheet.

Ocean Logic Pty Ltd
PO BOX 768 - Manly NSW 1655 - Australia
Tel: +61-2-99054152 Fax: +61-2-99050921
E-Mail: info@ocean-logic.com URL : http://www.ocean-logic.com/