On a Viterbi decoder design for low power dissipation.

(Master's Thesis)

Samir Ranpara and Dong S. Ha (Advisor)

VTVT Group (www.ee.vt.edu/ha/research)
Bradley Department of Electrical and Computer Engineering
Virginia Tech, Blacksburg, VA 24061
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(Abstract)

Convolutinal coding is a coding scheme often employed in deep space communications and recently in digital wireless communications. Viterbi decoders are used to decode convolutional codes. Viterbi decoders employed in digital wireless communications are complex and dissipates large power. With the proliferation of battery powered devices such as cellular phones and laptop computers, power dissipation, along with speed and area, is a major concern in VLSI design. In this thesis, we investigated a low-power design of Viterbi decoders for wireless communications applications. In CMOS technology the major source of power dissipation is attributed to dynamic power dissipation, which is due to the switching of signal values. The focus of our research in the low-power design of Viterbi decoders is reduction of dynamic power dissipation at logic level in the standard cell design environment. We considered two methods, clock-gating and toggle-filtering, in our design. A Viterbi decoder consists of five blocks. The clock-gating was applied to the survivor path storage block and the toggle-filtering to the trace-back block of a Viterbi decoder. We followed the standard cell design approach to implement the design. The behavior of a Viterbi decoder was described in VHDL, and then the VHDL description was modified to embed the low-power design. A gate level circuit was obtained from the behavioral description through logic synthesis, and a full scan design was incorporated into the gate level circuit to ease testing. The gate level circuit was placed and routed to generate a layout of the design. Our experimental result shows the proposed design

reduces the power dissipation of a Viterbi decoder by about 25 percent compared with the on without considering the low-power design.