Low-Power SRAM Compiler

- Automatically generates a static RAM for a given size. An array is partitioned into four blocks to reduce power dissipation.
- SKILL code is used to automate the layout.
- Leaf-cells were layout in full-custom.
  - SRAM Cell: a latch and two pass transistors
  - Sense amplifier: a cross-coupled differential amplifier
  - Decoder: pass transistor logic
  - Block selector: 2x4 decoder

Specification of 1Kx8 SRAM

- Technology: TSMC 0.35 \( \mu \)m
- Core size: 860 \( \mu \)m x 730 \( \mu \)m
- # of transistors: about 52,000
- Power dissipation: 37 mW at 3.3 V

<table>
<thead>
<tr>
<th></th>
<th>Original SRAM</th>
<th>Partitioned SRAM</th>
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</thead>
<tbody>
<tr>
<td><strong>Area (mm(^2)</strong></td>
<td>.406</td>
<td>.606</td>
</tr>
<tr>
<td><strong>Power (mW)</strong></td>
<td>67</td>
<td>37</td>
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</tbody>
</table>

Performance comparison

Layout of a partitioned SRAM