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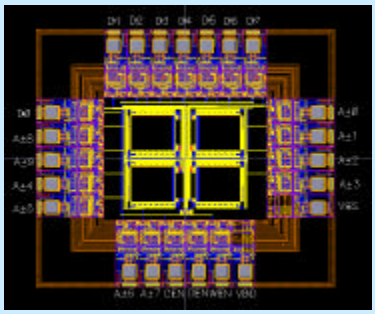
Low-Power SRAM Compiler

- **Automatically generates a static RAM for a given size. An array is partitioned into four blocks to reduce power dissipation.**
- **SKILL code is used to automate the layout.**
- **Leaf-cells were layout in full-custom.**
  - **SRAM Cell: a latch and two pass transistors**
  - **Sense amplifier: a cross-coupled differential amplifier**
  - **Decoder: pass transistor logic**
  - **Block selector: 2x4 decoder**

Specification of 1Kx8 SRAM

- **Technology: TSMC 0.35 μm**
- **Core size: 860 μm x 730 μm**
- **# of transistors: about 52,000**
- **Power dissipation: 37 mW at 3.3 V**
- **Performance comparison**

	Original SRAM	Partitioned SRAM
Area (mm^2)	.406	.606
Power (mW)	67	37



Layout of a partitioned SRAM