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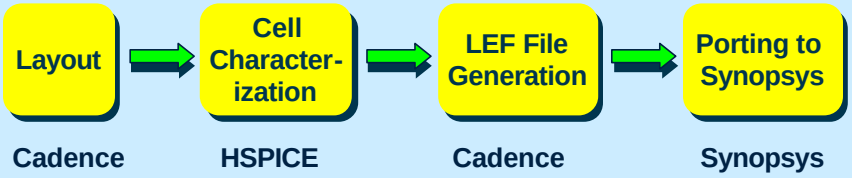
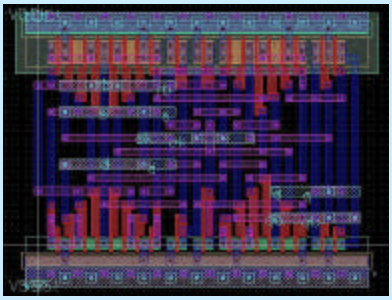
Low-Power Library Cells

- Development of low-power standard cell library to facilitate design of low-power system using high-level synthesis tools
- Target tools:
  - Simulation / Synthesis tool: Synopsys Design_Analyzer
  - Place-and-route tool: Cadence Silicon Ensemble
- Flow of Library Development:



Target Cells and Technology

- Static Complementary CMOS
  - Robustness
  - flexibility in power reduction strategy
- TSMC 0.25㎜, 2.5V, five metal layers
- Equalization of rise/fall delays for glitch reduction



D Flip-Flop with async. set-reset
size: 24.9´31.2㎜
Power: 219㎽ at 400MHz
Clock Capacitance: 29.5fF