Variable Resolution ADC

- Motivation: The power dissipation of an analog-to-digital converter (ADC) is proportional to the resolution, i.e., the number of bits.
- We proposed a variable resolution ADC whose resolution is determined dynamically according to the channel condition.

Specification of Our ADC

- Approach: The controller decides the number of bit cycles in the iterative ADC architecture.
- Specification:
  - Technology: TSMC 0.35 μm, triple metal layer
  - Resolution: 12 bits
  - Speed: 1.7 Mbps
  - Core Size: 430 μm x 300 μm