A STANDARD CELL LIBRARY FOR STUDENT PROJECTS

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www.ece.iit.edu/~cad

VLSI Computer Architecture, Arithmetic, and CAD Research Group (VCAAC)

0.50µ
0.25µ
0.18µ

Attractive Feature
Feature Sizes Available

Ease of Use:
Script Automated

sed
awk

IIT Standard-Cell Library

cadence
SYNOPSYS

Industry Standard
Software Supported

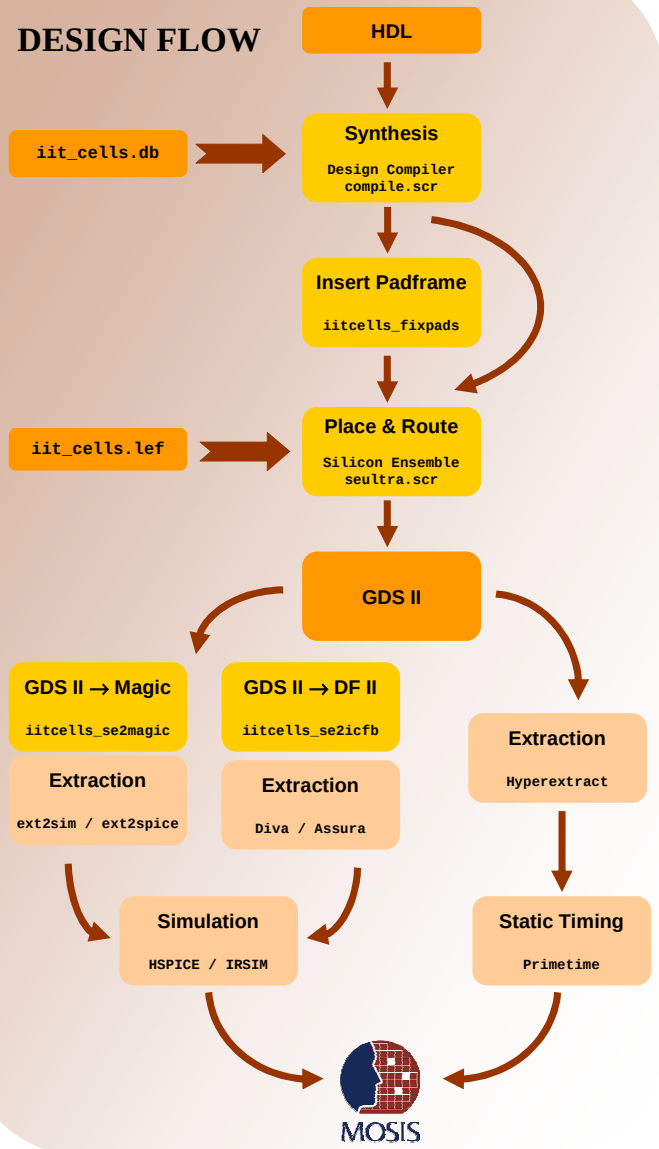
Fabrication: MOSIS
Educational Program

MOSIS

THE CELLS

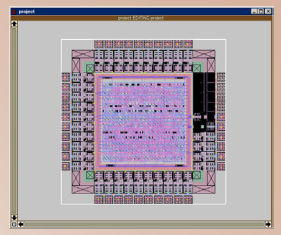
Simple Logic		2-Level Logic	
INV	(X1,X2,X4,X8)	AOI21	(X1)
NAND2/3	(X1)	AOI22	(X1)
NOR2/3	(X1)	OAI21	(X1)
XOR2	(X1)	OAI22	(X1)
XNOR2	(X1)	FA	(X1)
AND2	(X1,X2)	HA	(X1)
OR2X1	(X1,X2)	MUX2	(X1)
Buffers		**Sequential Logic**	
BUF	(X2,X4)	DFFNEG	(X1)
TBUF	(X1,X2)	DFFPOS	(X1)

DESIGN FLOW



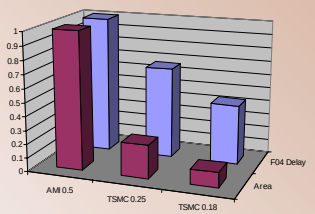
RESULTS

- Complete Standard-Cell Design Package
- Characterized for Timing and Power
- Script Automated
- Supports Padframe Synthesis
- Supports MOSIS Educational Program for Fabrication of Student Projects
- Supports Magic and ICFB
- Publicly available
  http://www.ece.iit.edu/~cad/scells



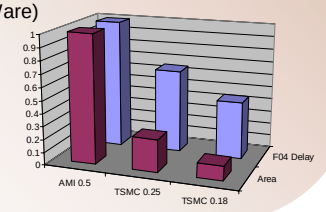
64 bit CLA (Hand coded)

Technology	F04 Delay [ns]	Area [mm²]
AMI 0.5µ	23.1	0.18
TSMC 0.25µ	15.4	0.04
TSMC 0.18µ	10.1	0.02



64 Bit Dadda Multiplier (Synopsys DesignWare)

Technology	F04 Delay [ns]	Area [mm²]
AMI 0.5µ	12.4	2.48
TSMC 0.25µ	8.0	0.62
TSMC 0.18µ	5.5	0.28



CELL DEVELOPMENT

Layout
Magic

Geometry Characterization
Cadence Abstract

Timing / Power Characterization
Cadence Signalstorm