but no heuristic particularly distinguishes itself from the pack.

Since clustering is still a very poorly understood realm of bipartitioning, we believe that seeking answers to the following questions will be important in future work:

- What is the correlation between clustering objectives and the effect of clusterings within two-phase FM? Is there a natural clustering objective for the two-phase FM application?
- What is the best number of clusters? In a hierarchical approach, how many clusters should be at each level and how many levels are needed?
- What is the best way to integrate a clustering or a series of clusterings into an FM-based algorithm (e.g., given a CPU resource in terms of the number of FM passes made, how should this resource be allocated)?
- What cluster size constraints should be imposed? Is it better to have balanced clusters (as advocated by [30]), or to have large clusters mixed with small ones (as in edge unclustering)?

We believe that once the answers to these questions are understood, the best clustering strategies will become evident.

7 Conclusions

The past several years have seen the field of netlist partitioning make numerous advances – in terms of new formulations and objectives for various specific applications, and in terms of new algorithmic approaches. This paper has surveyed these developments, with an emphasis on more recent ideas. Throughout our discussion, we have attempted to note the research directions that merit further investigation, but have also tried to avoid value judgements based on experimental results. In this concluding section, we offer a summary of the benchmarking techniques for graphs and circuits that have appeared in the literature; we end with a brief assessment of the more promising approaches seen in recent works, and possible future directions for the field.

7.1 Benchmarking

Many studies of partitioning are not specific to VLSI applications, or otherwise did not have any set of "real circuits" available for benchmarking. Thus, experiments have been conducted on various classes of random graphs, including:

- **Uniform:** A graph $G(n,p)$ has n vertices, with the edge between each pair of vertices independently present with probability p. Random graphs (and hypergraphs) have been used by e.g., [110] [187] [164]. See [26] for a review of graph-theoretic results established for this model.

- **Geometric:** The graph $U(n,d)$ [110] is generated by picking n random (x,y) coordinate pairs (corresponding to the n vertices) in the unit square, and introducing an edge between two vertices if the Euclidean distance between their corresponding (x,y) locations is no greater than d.

- **"Difficult" d-Regular:** A graph is in the class $G_{Bui}(n,b,d)$ if it has n vertices, is d-regular, and has expected optimum bisection width no greater than b. A construction was first given by Bui et al. [29], and a simpler variant construction was given in [83].

- **Bisection Specific:** A graph in the class of random graphs $G_{2set}(2n,p_1,p_2,bis)$ [30] has a given edge internal to n-vertex clusters C_1 and C_2 with probabilities p_1 and p_2, respectively. Exactly bis edges connect C_1 with C_2, with bis very likely to be the cost of the optimum bisection.

- **k-Way Specific:** The class $G_{Gar}(k,\frac{n}{k},p_i,p_e)$ [69] represents the multi-way extension of the Bisection Specific construction. A graph in this class has k clusters, each of size $\frac{n}{k}$; the $C(k,2)\cdot(\frac{n}{k})^2$ intracluster edges are each independently present with probability p_i, and the $k\cdot C(\frac{n}{k},2)$ intercluster edges are each independently present with probability p_e. See also such works as [1].

Other, more complex random constructions have also been proposed, e.g., [124] [161].

In recent years, works on netlist partitioning have begun using benchmark suites collected by ACM SIGDA for experimental comparisons.[14] Recently, the CAD Benchmarking Laboratory (CBL) at North Carolina State University has succeeded the Microelectronics Center of North Carolina as the host for maintaining and renewing suites of benchmarks (WWW: http://www.cbl.ncsu.edu/www/CBL_Home.html/ or ftp to ftp.cbl.ncsu.edu or email to benchmarks@cbl.ncsu.edu). The benchmarks that most commonly appear in experiments in the literature belong to the LayoutSynthesis90 and 92, ISCAS85 and 89 [121], and PDWorkshop93 suites; for FPGA partitioning, the Partitioning93 suite is typically used. All of these benchmarks were originally designed for either placement or synthesis, hence each experimenter must translate the benchmark to some usable partitioning format. The differences in interpretations of the benchmarks can lead to discrepancies in the resulting inputs, and researchers may end up comparing the cuts of graphs and hypergraphs that are not the same. For example, the number of modules reported for the Test02-06 benchmarks is higher in [195] than in [82], which is likely due to the interpretation of I/O pads. In other cases, problems may arise from netlist connectivity. For example, when converting the industry3.vpnr benchmark into PROUD format, the authors of GORDIAN observed

[14] Graphs from the Harwell-Boeing sparse matrix collection (anonymous ftp to orion.cerfacs.fr) have also appeared occasionally in the literature (e.g, [160]) and provide an excellent set of test cases for graph partitioning algorithms.

that the netlist was disconnected, and the smaller 27-module component was discarded since it had no external connections and since GORDIAN requires connections to I/O pads in order to place the circuit [155]. Other authors might not remove this smaller component, leading to different bisection and ratio cut results for the same algorithm and the "same" test case.

We believe that the VLSI partitioning field would greatly benefit from a standard set of benchmarks exclusively designed for partitioning. As a first step, TU Munich has made many benchmarks available in PROUD format [183] (WWW: http://www.regent.e-technik.tu-muenchen.de/) and we are currently making benchmarks available in a standard hypergraph format (WWW: http://ballade.cs.ucla.edu:8080/). Our group is currently working with TU Munich to ensure consistency between our formats, making either format suitable for comparisons. Clearly, such entities as the CBL are best equipped to take such efforts a step further, e.g., by constructing and propagating self-consistent translators among the many existing partitioning input formats. Such institutionalized uniformity will help to make future benchmarking results in the literature much more meaningful. At the same time, care must also be taken not to constrain research paths by removing useful information. As examples, (i) logic function information must be retained in order to explore logic-based replication or combined resynthesis and partitioning (cf. [22]), and (ii) directional information must be present in inputs to address acyclic, delay-minimization, etc. formulations.

By way of facilitating future comparisons, Table 1 lists various partitioning formulations, along with works that have provided experimental results for some of the standard benchmarks. These are of historical note, since formulations can become popular simply because of the existence of comparison data. For example, Riess et al. [156] were the first to present 19 benchmark results for the 45/55-constrained bipartitioning objective (i.e., $L = 0.45n$ and $U = 0.55n$). The objective is of interest since ratio cut solutions tend to be highly unbalanced and hence impractical, yet exact bisections are too restrictive. This work has very quickly become a standard object of comparisons (cf. [6] [94] [190]).

Many of the formulations listed in the Table are quite similar, e.g., the first five formulations are all bipartitioning variants. While it is unclear which formulation is "correct", all of the associated bipartitioning algorithms are certainly comparable in some sense. It remains for the field to establish a reasoned basis by which heuristic variants, and associated experimental results, can be evaluated. For instance, Hauck and Borriello [94] recently completed an excellent study of FM-based bipartitioning algorithms, yet their results do not use unit area (rather, they set $w(v) = deg(v) - 2$ for each $v \in V$). Although this unorthodox weighting scheme by no means invalidates their conclusions, it does complicate future extensions of their study vis-a-vis other works. We believe that whether to use area information, which balance constraints apply, etc. are issues that can be addressed by identifying benchmarks (or benchmark variants) that are particularly suited for specific formulations.

Objective	Papers
Ratio Cut (unit area)	[187] [80] [188] [48] [51] [156]
Ratio Cut (module area)	[51] [31]
45/55 Bipartitioning	[156] [190] [94] [6]
Bisection (unit area)	[94]
Bisection (module area)	[188] [82] [51] [176] [195]
FPGA Devices	[125] [126] [44] [100] [38] [157]
Scaled Cost	[37] [3] [5] [4] [6]
Cluster Ratio	[3] [193]
Multi-Way + slack (module area)	[49] [194]
Multi-way + slack (unit area)	[79] [8]
Multi-way balanced	[11]
Min-Delay Clustering	[140] [45] [151] [191]
Absorption	[179] [4]
DS	[82] [4]
Density	[101]
Replication	[122] [104]
MCM/Quadrisection	[178] [159] [158]

Table 1: Various partitioning formulations and some works that provide corresponding experimental results.

Another weakness in the present "comparison-based literature" stems from having non-standard implementations of traditional algorithms, e.g., many researchers (including ourselves) have implemented their own FM-based 2-way or multi-way partitioners. On the other hand, Section 3 observed that subtle differences in implementation can have very large effects on solution quality. Widespread availability of canonical, well-tested implementations of standard algorithms (e.g., through CBL) could alleviate this problem. Also, researchers could perhaps use a shared site to make their source codes and/or executables available, to facilitate future comparisons as more benchmarks become available.[15] Authors of future work might also provide detailed descriptions of their experimental protocols and benchmark instances, since so many discrepancies are possible.

Finally, there are many deeper questions associated with the use of benchmarks in the VLSI partitioning literature (cf. panel discussions at many leading conferences in recent years). The beginnings of a list might include:

- Is it correct, as has been the case in recent years, to equate "progress" with "beating" previous results in terms of both solution quality and run-time? Arguably, this heavily biases against

[15] There are instructive precedents in the fields of combinatorial optimization and operations research. For example, WWW http://netlib.att.com provides a repository for mathematical software and related items, including eigenvector computations, mathematical programming and network flow packages, etc. Similarly, the OR-Library at the Imperial College Management School (WWW http://mscmga.ms.ic.ac.uk/info.html) gives a collection of test data sets for a variety of combinatorial formulations including LP, IP, QAP and matching (but not yet partitioning). Another type of impetus comes from regular "challenges" within the field (cf. the ACM Physical Design Workshop placement challenges from 1987-1991, the recent DIMACS Challenges in combinatorial optimization, etc.).

such novel approaches as evolutionary computing, parallel search, parallel annealing, constraint satisfaction, etc. Experimental setup, data collection and reporting methodology, etc. will also affect the perception of superiority. Furthermore, the present trend may well be responsible for the recent proliferation of "new formulations" for which there are no previous results that must be "beaten".

- Is it wise for the field to focus, as it has in recent years, on results for "real-world", as opposed to "artificial", instances? Note that (i) the provenance and functionality of benchmarks are often "sanitized" away so that it is unclear whether the benchmarks are representative; (ii) optimal solutions are never known for real-world instances (see [87] for a partial workaround); and (iii) any benchmark suite (as opposed to a generator for a class of (random) instances) is limited in size, which can in turn limit the significance of comparisons.

- Should industry users of CAD algorithms be more forthcoming with real-world test cases? Note that the literature for, e.g., the Multi-Way FPGA Device formulation [44] [100] includes test cases that presently can be obtained only under a signed nondisclosure agreement.

7.2 Perspectives

We conclude our work by listing what we consider to be promising directions for future research.

First, we believe that move-based approaches such as iterative improvement, stochastic hill-climbing, or evolutionary optimization are increasingly attractive. Certainly, FM and its derivatives have comprised the partitioning state-of-the-art throughout all areas of VLSI CAD during the past decade. However, small differences in implementations can lead to large differences in solution quality.[16] It seems worthwhile to continue to explore various implementations and tie-breaking strategies, especially given the large payoffs that can result from only minor code changes.

Second, we have noted that in practice, move-based approaches are often run many times with different *random* starting solutions. However, adapting the starting point based on knowledge from prior iterations can more quickly lead to stable solution quality; such an "adaptive multi-start" approach shares characteristics with hybrid genetic-local search techniques in evolutionary optimization. The paradigm of evolutionary optimization, with its unique style of search in the solution space, has claimed successes in the arenas of operations research and combinatorial optimization, which bodes well for future application to VLSI partitioning.

Third, spectral approaches that utilize multiple eigenvectors appear promising. Previous spectral

[16] Such studies can call into question the conclusions drawn in oft-cited works, in this case those of [123] [164] [189] regarding "lookahead" in iterative improvement strategies.

approaches that associate a single eigenvector with a cluster [18] or use only one eigenvector [80] may have inherent limitations. Works such as [68] [6] achieve solutions by associating a partitioning instance with the vector space comprised by multiple eigenvectors, yet heuristics for this representation are largely undeveloped. In addition, older spectral ideas may be worth revisiting, e.g., Donath and Hoffman [59] suggested varying the degree matrix to obtain better eigenvectors.

Fourth, finding good 1-dimensional circuit representations, (i.e., linear orderings of the modules) also seems promising. Dynamic programming can optimally split such an ordering into multiple clusters with respect to many standard objectives. Also, analytic techniques such as conjugate gradient method methods and successive over relaxation are naturally 1-dimensional. Finally, different methods for producing a partitioning from a linear ordering (such as the PARABOLI approach of gradually pulling apart an ordering while reoptimizing it) merit further investigation.

Fifth, we note that three trends – (i) the need to address highly constrained and complex formulations (e.g., timing, I/O, clock period, etc. constraints), (ii) the increased transfer of algorithm techniques from other well-established disciplines, and (iii) the availability of more computing power for CAD optimizations – combine to make combinatorial techniques increasingly viable. Analogous to the rediscovery of spectral and flow computations in recent years, we believe that approaches based on mathematical programming – including implicit enumeration methods such as branch-and-bound solution of ILP formulations – will be a "growth area" in VLSI partitioning.

Sixth, clustering now seems a required extension to many existing algorithms in light of increasing problem complexity. New criteria for clustering, as well as definitive studies correlating performance of the two-phase FM mechanism and the underlying clustering strategy, are still needed. Alternatives to the two-phase methodology are also well worth exploring. Works such as [94] provide important first steps in this direction.

Finally, we have noted that the recent literature contains many heuristic forays and new problem variations, which is not unexpected when many new works are essentially evaluated by the numbers they achieve for a limited suite of (outdated) test cases. In the previous subsection, we sketched a wish list for the future which includes: (i) canonical algorithm implementations (e.g., of the KL and FM heuristics) for comparison, and more widespread conformity with standard benchmark interchange formats, (ii) larger, public benchmarks with more functional and library information, (iii) public availability of partitioning codes, test instances, and actual partitioning solutions used in reported results, (iv) elimination of biases against nascent "future algorithm technologies" which may not yet be competitive in terms of both solution quality and efficiency, (v) more creative criteria for algorithms (cf. the "self-scaling" concept in [87]), and (vi) more complete descriptions of experimental protocols, along with more statistically meaningful data. These may be the most important future directions for researchers in VLSI partitioning, as we strive to achieve increased relevance to current design practice, and a more reasoned, long-term, and scientific approach to this intractable problem.

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References

[1] D. H. Ackley. *A Connectionist Machine for Genetic Hillclimbing.* Kluwer, 1987.

[2] R. K. Ahuja, T. L. Magnanti, and J. B. Orlin. *Network Flows: Theory, Algorithms, and Applications.* Prentice Hall, 1993.

[3] C. J. Alpert and A. B. Kahng. Geometric embeddings for faster and better multi-way netlist partitioning. In *Proc. ACM/IEEE Design Automation Conf.*, pages 743–748, 1993.

[4] C. J. Alpert and A. B. Kahng. A general framework for vertex orderings, with applications to netlist clustering. In *Proc. IEEE Intl. Conf. Computer-Aided Design*, pages 63–67, 1994.

[5] C. J. Alpert and A. B. Kahng. Multi-way partitioning via spacefilling curves and dynamic programming. In *Proc. ACM/IEEE Design Automation Conf.*, pages 652–657, 1994.

[6] C. J. Alpert and S. Z. Yao. Spectral partitioning: the more eigenvectors, the better. In *Proc. ACM/IEEE Design Automation Conf. (to appear)*, 1995.

[7] A. A. Andreatta and C. C Ribeiro. A graph partitioning heuristic for the parallel pseudo-exhaustive logical test of vlsi combinational circuits. *Annals of Operations Research*, 50:1–36, 1994.

[8] S. Areibi and A. Vannelli. Advanced search techniques for circuit partitioning. In *DIMACS Series in Discrete Mathematics and Theoretical Computer Science*, pages 77–98, 1993.

[9] S. Areibi and A. Vannelli. Circuit partitioning using a tabu search approach. In *Proc. IEEE Intl. Symp. Circuits and Systems*, pages 1643–1646, 1993.

[10] S. Areibi and A. Vannelli. A combined eigenvector tabu search approach for circuit partitioning. In *Custom Integrated Circuits Conf.*, pages 9.7.1–9.7.4, 1993.

[11] S. Areibi and A. Vannelli. An efficient solution to circuit partitioning using tabu search and genetic algorithms. In *6th Int Conference of Micro Electronics*, pages 70–74, Istanbul, 1994.

[12] K. S. Arun and V. B. Rao. Two-way graph partitioning by principal components. In *Proc. IEEE Intl. Symp. Circuits and Systems*, pages 2877–2880, 1990.

[13] K. S. Arun and V. B. Rao. New heuristics and lower bounds for graph partitioning. In *Proc. IEEE Intl. Symp. Circuits and Systems*, pages 1172–1175, 1991.

[14] B. Awerbuch and T. Leighton. Multicommodity flows: A survey of recent research. In *4th Intl. Symp. Algorithms and Computation*, pages 297–302, 1993.

[15] H. B. Bakoglu. *Circuits, Interconnections, and Packaging for VLSI.* Addison-Wesley Pub. Co., 1990.

[16] C. F. Ball, P. V. Kraus, and D. A. Mlynski. Fuzzy partitioning applied to vlsi-floorplanning and placement. In *Proc. IEEE Intl. Symp. Circuits and Systems*, pages 177–180, 1994.

[17] S. T. Barnard and H. D. Simon. A fast multilevel implementation of recursive spectral bisection for partitioning unstructured problems. Technical Report RNR-92-033, NASA Ames, November 1992.

[18] E. R. Barnes. An algorithm for partitioning the nodes of a graph. *SIAM Journal of Algebraic and Discrete Methods*, 3(4):541–550, 1982.

[19] E. R. Barnes, A. Vannelli, and J. Q. Walker. A new heuristic for partitioning the nodes of a graph. *SIAM J. Disc. Math.*, 1(3):299–305, 1988.

[20] J. J. Bartholdi and L. K. Platzman. Heuristics based on spacefilling curves for combinatorial problems in euclidean space. *Management Sciences*, 34(3):291–305, 1988.

[21] E. B. Baum. Iterated descent: A better algorithm for local search in combinatorial optimization problems. In D. Touretzky, editor, *Proc. Neural Information Processing Systems*, November 1988.

[22] M. Beardslee and A. Sangiovanni-Vincentelli. An algorithm for improving partitions of pin-limited multi-chip systems. In *Proc. IEEE Intl. Conf. Computer-Aided Design*, pages 378–385, 1993.

[23] C. Berge. *Graphs and Hypergraphs*. American Elsevier, New York, 1976.

[24] J. Blanks. Near-optimal placement using a quadratic objective function. In *Proc. ACM/IEEE Design Automation Conf.*, pages 609–615, 1985.

[25] K. Boese, A. Kahng, and S. Muddu. A new adaptive multi-start technique for combinatorial global optimizations. *Operations Research Letters*, 16:101–113, 1994.

[26] B. Bollobas. *Random Graphs*. Academic Press, 1985.

[27] R. B. Boppana. Eigenvalues and graph bisection: An average-case analysis. In *Proc. IEEE Symp. Foundations of Computer Science*, pages 280–285, 1987.

[28] R. Brayton, G. Hachtel, C. McMullen, and A. Sangiovanni-Vincentelli. *Logic Minimization Algorithms for VLSI Synthesis*. Kluwer, 1985.

[29] T. Bui, S. Chaudhuri, T. Leighton, and M. Sipser. Graph bisection algorithms with good average case behavior. *Combinatorica*, 7(2):171–191, 1987.

[30] T. Bui, C. Heigham, C. Jones, and T. Leighton. Improving the performance of the kernighan-lin and simulated annealing graph bisection algorithms. In *Proc. ACM/IEEE Design Automation Conf.*, pages 775–778, 1989.

[31] T. N. Bui and B. R. Moon. A fast and stable hybrid genetic algorithm for the ratio-cut partitioning problem on hypergraphs. In *Proc. ACM/IEEE Design Automation Conf.*, pages 664–669, 1994.

[32] T. N. Bui and B. R. Moon. A genetic algorithm for a special class of the quadratic assignment problem. In *DIMACS Series in Discrete Mathematics and Theoretical Computer Science*, volume 16, pages 99–116, 1994.

[33] T. Bultan and C. Aykanat. Circuit partitioning using parallel mean field annealing algorithms. In *IEEE Symp. Parallel and Distributed Processing*, pages 534–541, 1991.

[34] R. E. Burkard and T. Bonniger. A heuristic for quadratic boolean programs with applications to quadratic assignment. *European Journal of Operational Research*, 13:372–386, 1983.

[35] R. L. Cannon, J. V. Dave, and J. C. Bezdek. Efficient implementation of the fuzzy c-means clustering algorithms. *IEEE Trans. Pattern Analysis and Machine Intelligence*, 8(2), March 1986.

[36] R. C. Carden and C.-K. Cheng. A global router using an efficient approximate multicommodity multi-terminal flow algorithm. In *Proc. ACM/IEEE Design Automation Conf.*, pages 316–321, 1991.

[37] P. K. Chan, M. D. F. Schlag, and J. Y. Zien. Spectral k-way ratio-cut partitioning and clustering. *IEEE Trans. Computer-Aided Design*, 13(8):1088–1096, 1994.

[38] P. K. Chan, M. D. F. Schlag, and J. Y. Zien. Spectral-based multi-way fpga partitioning. In *Proc. ACM/SIGDA International Workshop on Field-Programmable Gate Arrays*, pages 133–139, 1995.

[39] R. Chandrasekharam, S. Subhramanian, and S. Chaudhury. Genetic algorithm for node partitioning problem and applications in vlsi design. *IEE Proceedings E (Computers and Digital Techniques)*, 140(5):255–60, September 1993.

[40] H. R. Charney and D. L. Plato. Efficient partitioning of components. In *Proc. Design Automation Workshop*, pages 16–0 – 16–21, 1968.

[41] A. C. Chatterjee and R. Hartley. A new simultaneous circuit partitioning and chip placement approach based on simulated annealing. In *Proc. ACM/IEEE Design Automation Conf.*, pages 36–39, 1990.

[42] Y.-P. Chen, T.-C. Wang, and D. F. Wong. A graph partitioning problem for multiple-chip design. In *Proc. IEEE Intl. Symp. Circuits and Systems*, pages 1778–1781, 1993.

[43] C. K. Cheng. The optimal partitioning of networks. *Networks*, 22:297–315, 1992.

[44] N.-C. Chou, L.-T. Liu, C.-K. Cheng, W.-J. Dai, and R. Lindelof. Circuit partitioning for huge logic emulation systems. In *Proc. ACM/IEEE Design Automation Conf.*, pages 244–249, 1994.

[45] J. Cong and Y. Ding. An optimal technology mapping algorithm for delay optimization in lookup-table based fpga designs. In *Proc. IEEE Intl. Conf. Computer-Aided Design*, pages 48–53, 1992.

[46] J. Cong and Y. Ding. On area/depth trade-off in lut-based fpga technology mapping. In *Proc. ACM/IEEE Design Automation Conf.*, pages 213–218, 1993.

[47] J. Cong, L. Hagen, and A. B. Kahng. Random walks for circuit clustering. In *Proc. IEEE Intl. ASIC Conf.*, pages 14.2.1–14.2.4, 1991.

[48] J. Cong, L. Hagen, and A. B. Kahng. Net partitions yield better module partitions. In *Proc. ACM/IEEE Design Automation Conf.*, pages 47–52, 1992.

[49] J. Cong, W. Labio, and N. Shivakumar. Multi-way vlsi circuit partitioning based on dual net representation. In *Proc. IEEE Intl. Conf. Computer-Aided Design*, pages 56–62, 1994.

[50] J. Cong, Z. Li, and R. Bagrodia. Acyclic multi-way partitioning of boolean networks. In *Proc. ACM/IEEE Design Automation Conf.*, pages 670–675, 1994.

[51] J. Cong and M'L. Smith. A parallel bottom-up clustering algorithm with applications to circuit partitioning in vlsi design. In *Proc. ACM/IEEE Design Automation Conf.*, pages 755–760, 1993.

[52] A. Dasdan and C. Aykanat. Improved multiple-way circuit partitioning algorithms. In *Proc. ACM/SIGDA International Workshop on Field-Programmable Gate Arrays*, 1994.

[53] H. L. Davidson and E. Kelly, July 1993. Personal communication.

[54] D. E. Van den Bout and T. K. Miller III. Graph partitioning using annealed neural networks. *IEEE Transaction on Neural Networks*, 1(2):192–203, 1990.

[55] S. Dey, F. Brglez, and G. Kedem. Corolla based circuit partitioning and resynthesis. In *Proc. ACM/IEEE Design Automation Conf.*, pages 607–612, 1990.

[56] S. Dey, F. Brglez, and G. Kedem. Partitioning sequential circuits for logic optimization. In *Proc. IEEE Intl. Conf. Computer Design*, pages 70–76, 1990.

[57] W. E. Donath. Placement and average interconnection lengths of computer logic. *IEEE Trans. Circuits and Systems*, CAS-26(4):272–277, 1979.

[58] W. E. Donath. Logic partitioning. In B. Preas and M. Lorenzetti, editors, *Physical Design Automation of VLSI Systems*, pages 65–86. Benjamin/Cummings, 1988.

[59] W. E. Donath and A. J. Hoffman. Lower bounds for the partitioning of graphs. *IBM J. Res. Develop.*, 17(5):420–425, 1973.

[60] A. E. Dunlop and B. W. Kernighan. A procedure for layout of standard-cell vlsi circuits. *IEEE Trans. Computer-Aided Design*, 4(1):92–98, 1985.

[61] S. Dutt. New faster kernighan-lin-type graph-partitioning algorithms. In *Proc. IEEE Intl. Conf. Computer-Aided Design*, pages 370–377, 1993.

[62] J. Fan, B. Catanzaro, C. K. Cheng, and S. H. Lee. Partitioning of opto-electronic multichip modules. In *Proc. IEEE Multi-Chip Module Conf.*, pages 138–143, 1994.

[63] T. A. Feo and M. Khellaf. A class of bounded approximation algorithms for graph partitioning. *Networks*, 20:181–195, 1990.

[64] M. Feuer. Connectivity of random logic. *IEEE Trans. Computers*, C-31(1):29–33, January 1982.

[65] C. M. Fiduccia and R. M. Mattheyses. A linear time heuristic for improving network partitions. In *Proc. ACM/IEEE Design Automation Conf.*, pages 175–181, 1982.

[66] L. R. Ford, Jr. and D. R. Fulkerson. *Flows in Networks.* Princeton University Press, 1962.

[67] J. Frankle. *Circuit Placement Methods Using Multiple Eigenvectors and Linear Probe Techniques.* PhD thesis, UC Berkeley, 1987.

[68] J. Frankle and R. M. Karp. Circuit placement and cost bounds by eigenvector decomposition. In *Proc. IEEE Intl. Conf. Computer-Aided Design*, pages 414–417, 1986.

[69] J. Garbers, H. J. Promel, and A. Steger. Finding clusters in vlsi circuits. In *Proc. IEEE Intl. Conf. Computer-Aided Design*, pages 520–523, 1990.

[70] M. Garey and D. S. Johnson. *Computers and Intractability: A Guide to the Theory of NP-Completeness.* Freeman, 1979.

[71] C. H. Gebotys and M. I. Elmasry. *Optimal VLSI Architectural Synthesis: Area, Performance, and Testability.* Kluwer, 1992.

[72] S. Geman and D. Geman. Stochastic relaxation, gibbs distributions, and the bayesian restoration of images. *IEEE Trans. Pattern Analysis and Machine Intelligence*, 6:721–741, 1984.

[73] P. E. Gill, W. Murray, and M. H. Wright. *Practical Optimization.* Academic Press, 1981.

[74] F. Glover. Tabu search - part i. *ORSA Journal on Computing*, 1:190–206, 1989.

[75] A. V. Goldberg, É. Tardos, and R. E. Tarjan. Network flow algorithms. Technical Report STAN-CS-89-1252, Stanford University CS Dept., 1989.

[76] M. K. Goldberg and M. Burstein. Heuristic improvement technique for bisection of vlsi networks. In *Proc. IEEE Intl. Conf. Computer Design*, pages 122–125, 1983.

[77] R. Gomory and T. C. Hu. Multi-terminal network flows. *J. SIAM*, 9:551–570, 1961.

[78] J. W. Greene and K. J. Supowit. Simulated annealing without rejected moves. In *Proc. IEEE Intl. Conf. Computer Design*, pages 658–663, 1984.

[79] S. W. Hadley, B. L. Mark, and A. Vannelli. An efficient eigenvector approach for finding netlist partitions. *IEEE Trans. Computer-Aided Design*, 11(7):885–892, 1992.

[80] L. Hagen and A. B. Kahng. Fast spectral methods for ratio cut partitioning and clustering. In *Proc. IEEE Intl. Conf. Computer-Aided Design*, pages 10–13, 1991.

[81] L. Hagen and A. B. Kahng. Improving the quadratic objective function in module placement. In *Proc. IEEE Intl. ASIC Conf.*, pages 42–45, 1992.

[82] L. Hagen and A. B. Kahng. A new approach to effective circuit clustering. In *Proc. IEEE Intl. Conf. Computer-Aided Design*, pages 422–427, 1992.

[83] L. Hagen and A. B. Kahng. New spectral methods for ratio cut partitioning and clustering. *IEEE Trans. Computer-Aided Design*, 11(9):1074–1085, 1992.

[84] L. Hagen and A. B. Kahng. Combining problem reduction and adaptive multi-start: A new technique for superior iterative partitioning. *IEEE Trans. Computer-Aided Design (to appear)*, 1993.

[85] L. Hagen, A. B. Kahng, F. J. Kurdahi, and C. Ramachandran. On the intrinsic rent parameter and spectra-based partitioning methodologies. *IEEE Trans. Computer-Aided Design*, 13(1):27–37, 1994.

[86] L. W. Hagen, D. J.-H. Huang, and A. B. Kahng. On implementation choices for iterative improvement partitioning algorithms. *IEEE Trans. Computer-Aided Design (submitted)*, 1995.

[87] L. W. Hagen, D. J.-H. Huang, and A. B. Kahng. Quantified suboptimality of vlsi layout heuristics. *IEEE Trans. Computer-Aided Design (to appear)*, 1995.

[88] B. Hajek. Cooling schedules for optimal annealing. *Mathematics of Operations Research*, 13(2):311–329, 1988.

[89] K. M. Hall. An r-dimensional quadratic placement algorithm. *Management Science*, 17:219–229, 1970.

[90] T. Hamada, C.-K. Cheng, and P. M. Chau. A wire length estimation technique utilizing neighborhood density equations. In *Proc. ACM/IEEE Design Automation Conf.*, pages 57–61, 1992.

[91] M. Hanan, P. K. Wolff, and B. J. Agule. A study of placement techniques. *J. Design Automation and Fault-Tolerant Computing*, 2:28–61, 1978.

[92] J. Hao and J. B. Orlin. A faster algorithm for finding the minimum cut in a graph. In *Proc. ACM/SIAM Symp. Discrete Algorithms*, pages 165–174, Orlando, January 1992.

[93] N. Hasan and C. L. Liu. Minimum fault coverage in reconfigurable arrays. In *IEEE Intl. Symp. on Fault-Tolerant Computing Systems*, pages 248–353, 1988.

[94] S. Hauck and G. Borriello. An evaluation of bipartitioning techniques. In *Proc. Chapel Hill Conf. on Adv. Research in VLSI (to appear)*, 1995.

[95] S. Hauck and G. Borriello. Logic partition orderings for multi-fpga systems. In *Proc. ACM/SIGDA International Workshop on Field-Programmable Gate Arrays*, pages 32–38, 1995.

[96] B. Hendrickson and R. Leland. An improved spectral graph partitioning algorithm for mapping parallel computations. Technical report, Sandia National Laboratories, September 1992.

[97] A. G. Hoffman. The dynamic locking heuristic – a new graph partitioning algorithm. In *Proc. IEEE Intl. Symp. Circuits and Systems*, pages 173–176, 1994.

[98] J. Holland. *Adaptation in Natural and Artificial Systems.* University of Michigan Press, 1975.

[99] T. C. Hu and K. Moerder. Multiterminal flows in a hypergraph. In T. C. Hu and E. Kuh, editors, *VLSI Circuit Layout: Theory and Design*, pages 87–93. IEEE Press, 1985.

[100] D. J.-H. Huang and A. B. Kahng. Multi-way system partitioning into single or multiple type fpgas. In *Proc. ACM/SIGDA International Workshop on Field-Programmable Gate Arrays*, pages 140–145, 1995.

[101] D. J.-H. Huang and A. B. Kahng. When clusters meet partitions: New density-based methods for circuit decomposition. In *Proc. European Design and Test Conf. (to appear)*, March 1995.

[102] M. Hulin. Circuit partitioning with genetic algorithms using a coding scheme to preserve the structure of the circuit. In *Parallel Problem Solving from Nature*, pages 75–79. Springer-Verlag, 1990.

[103] J. Hwang and A. El Gamal. Optimal replication for min-cut partitioning. In *ICCAD*, pages 432–435, 1992.

[104] J. Hwang and A. El Gamal. Optimal replication for min-cut partitioning. *IEEE Trans. Computer-Aided Design*, 14(1):96–106, 1995.

[105] T.-T. Hwang, R. M. Owens, and M. J. Irwin. Exploiting communication complexity for multilevel logic synthesis. *IEEE Trans. Computer-Aided Design*, 9(10):1017–1027, October 1990.

[106] E. Ihler, D. Wagner, and F. Wagner. Modeling hypergraphs by graphs with the same mincut properties. *Information Processing Letters*, 45(4):171–175, March 1993.

[107] S. Iman, M. Pedram, C. Fabian, and J. Cong. Finding uni-directional cuts based on physical partitioning and logic restructuring. In *Proc. ACM/SIGDA Physical Design Workshop*, pages 187–198, Los Angeles, 1993.

[108] H. Inayoshi and B. Manderick. The weighted graph bi-partitioning problem: A look at ga performance. In *Parallel Problem Solving from Nature*, pages 617–625. Springer-Verlag, 1992.

[109] D. S. Johnson. Local optimization and the traveling salesman problem. In *Proc. of the 17th Intl. Colloquium on Automata, Languages and Programming*, pages 446–460, July 1990.

[110] D. S. Johnson, C. R. Aragon, L. A. McGeoch, and C. Schevon. Optimization by simulated annealing: An experimental evaluation part i, graph partitioning. *Operations Research*, 37:865–892, 1989.

[111] S. C. Johnson. Hierarchical clustering schemes. *Psychometrika*, 32(3):241–254, 1967.

[112] A. B. Kahng. Fast hypergraph partition. In *Proc. ACM/IEEE Design Automation Conf.*, pages 762–766, 1989.

[113] Y. Kamidoi, S. Wakabayashi, J. Miyao, and N. Yoshida. A fast heuristic for hypergraph bisection. In *Proc. IEEE Intl. Symp. Circuits and Systems*, volume 2, pages 1160–1163, 1991.

[114] D. Karger. Global min-cuts in rnc, and other ramifications of a simple min-cut algorithm. In *Proc. ACM/SIAM Symp. Discrete Algorithms*, pages 21–30, 1993.

[115] H. Karloff. *Linear programming*. Birkhauser, 1991.

[116] S. Kauffman and S. Levin. Toward a general theory of adaptive walks on rugged landscapes. *J. Theoretical Biology*, 128:11–45, 1987.

[117] B. W. Kernighan and S. Lin. An efficient heuristic procedure for partitioning graphs. *Bell Syst. Tech. J.*, 49(2):291–307, 1970.

[118] S. Khan and V. Madisetti. Yield-based system partitioning strategies for mcm and sem design. In *Proc. IEEE Intl. Symp. Circuits and Systems*, pages 144–149, 1994.

[119] S. Kirkpatrick, C. D. Gelatt, Jr., and M. P. Vecchi. Optimization by simulated annealing. *Science*, 220:671–680, 1983.

[120] J. M. Kleinhans, G. Sigl, F. M. Johannes, and K. J. Antreich. GORDIAN: VLSI placement by quadratic programming and slicing optimization. *IEEE Trans. Computer-Aided Design*, 10(3):356–365, 1991.

[121] K. Kozmiński. Benchmarks of layout synthesis – evolution and current status. In *Proc. ACM/IEEE Design Automation Conf.*, pages 265–270, 1991.

[122] C. Kring and A. R. Newton. A cell-replicating approach to mincut-based circuit partitioning. In *Proc. IEEE Intl. Conf. Computer-Aided Design*, pages 2–5, 1991.

[123] B. Krishnamurthy. An improved min-cut algorithm for partitioning VLSI networks. *IEEE Trans. Computers*, 33(5):438–446, 1984.

[124] B. Krishnamurthy. Constructing test cases for partitioning heuristics. *IEEE Trans. Computers*, C-36(9):1112–1114, September 1987.

[125] R. Kužnar, F. Brglez, and K. Kozminski. Cost minimization of partitions into multiple devices. In *Proc. ACM/IEEE Design Automation Conf.*, pages 315–320, 1993.

[126] R. Kužnar, F. Brglez, and B. Zajc. Multi-way netlist partitioning into heterogeneous fpgas and minimization of total device cost and interconnect. In *Proc. ACM/IEEE Design Automation Conf.*, pages 238–243, 1994.

[127] P. J. M. Laarhoven and E. H. L. Aarts. *Simulated Annealing: Theory and Applications*. D.Reidel, Boston, 1987.

[128] B. Landman and R. Russo. On a pin versus block relationship for partition of logic graphs. *IEEE Trans. Computers*, C-20:1469, 1971.

[129] E. L. Lawler. *Combinatorial Optimization: Networks and Matroids*. Holt, Rinehart, and Winston, 1976.

[130] E. L. Lawler, K. N. Levitt, and J. Turner. Module clustering to minimize delay in digital networks. *IEEE Trans. Computers*, 18:47–57, 1969.

[131] T. Leighton, F. Makedon, and S. Tragoudas. Approximation algorithms for VLSI partition problems. In *Proc. IEEE Intl. Symp. Circuits and Systems*, pages 2865–2868, 1990.

[132] T. Leighton and S. Rao. An approximate max-flow min-cut theorem for uniform multicommodity flow problems with applications to approximation algorithms. In *Proc. IEEE Symp. Foundations of Computer Science*, pages 422–431, 1988.

[133] T. Lengauer. *Combinatorial Algorithms for Integrated Circuit Layout.* Wiley-Teubner, 1990.

[134] A. Lim and Y.-M. Chee. Graph partitioning using tabu search. In *Proc. IEEE Intl. Symp. Circuits and Systems*, pages 1164–7, 1991.

[135] L. T. Liu, M. T. Kuo, C. K. Cheng, and T. C. Hu. A replication cut for two-way partitioning. *IEEE Trans. Computer-Aided Design (to appear)*, 1995.

[136] L. T. Liu, M. Shih, and C.-K. Cheng. Data flow partitioning for clock period and latency minimization. In *Proc. ACM/IEEE Design Automation Conf.*, pages 658–663, 1994.

[137] L. T. Liu, M. Shih, N.-C. Chou, C.-K. Cheng, and W. Ku. Performance driven partitioning using retiming and replication. In *Proc. IEEE Intl. Conf. Computer-Aided Design*, pages 296–299, 1993.

[138] D. W. Matula and F. Shahrokhi. The maximum concurrent flow problem and sparsest cuts. Technical report, Southern Methodist Univ., March 1986.

[139] B. Mohar. The laplacian spectrum of graphs. In Y. Alavi and et al., editors, *Graph Theory, Combinatorics, and Applications*, pages 871–898. Wiley, 1991.

[140] R. Murgai, R. K. Brayton, and A. Sangiovanni-Vincentelli. On clustering for minimum delay/area. In *Proc. IEEE Intl. Conf. Computer-Aided Design*, pages 6–9, 1991.

[141] H. Nagamochi and T. Ibaraki. Computing edge-connectivity in multigraphs and capacitated graphs. *Siam Journal of Discrete Mathematics*, 5(1):54–66, 1992.

[142] A. R. Newton, April 1991. Personal communication.

[143] T.-K. Ng, J. Oldfield, and V. Pitchumani. Improvements of a mincut partition algorithm. In *Proc. IEEE Intl. Conf. Computer-Aided Design*, pages 479–473, 1987.

[144] C.-I. Park and Y.-B. Park. An efficient algorithm for vlsi network partitioning problem using a cost function with balancing factor. *IEEE Trans. Computer-Aided Design*, 12(11):1686–1694, 1993.

[145] C. Peterson and J. R. Anderson. Neural networks and np-complete optimization problems; a performance study on the graph bisection problem. *Complex Systems*, 2(1):59–89, February 1988.

[146] L. T. Pillage and R. A. Rohrer. A quadratic metric with a simple solution scheme for initial placement. In *Proc. ACM/IEEE Design Automation Conf.*, pages 324–329, 1988.

[147] S. Pissanetsky. *Sparse Matrix Technology.* Academic Press, 1984.

[148] A. Pothen, H. D. Simon, and K. P. Liou. Partitioning sparse matrices with eigenvectors of graphs. *SIAM J. Matrix Analysis and its Applications*, 11:430–452, 1990.

[149] B. T. Preas and M. J. Lorenzetti, editors. *Physical Design Automation of VLSI Systems.* Benjamin/Cummings, 1988.

[150] F. P. Preparata and M. I. Shamos. *Computational Geometry: An Introduction.* Springer-Verlag, New York, 1985.

[151] R. Rajaraman and D. F. Wong. Optimal clustering for delay minimization. In *Proc. ACM/IEEE Design Automation Conf.*, pages 309–314, 1993.

[152] C. R. Rao. The use and interpretation of principal component analysis in applied research. *Sankhya Series A*, 26:329–358, 1964.

[153] M. Razaz. A fuzzy c-means clustering placement algorithm. In *Proc. IEEE Intl. Symp. Circuits and Systems*, pages 2051–2054, 1993.

[154] F. Rendl and H. Wolkowicz. A projection technique for partitioning the nodes of a graph. Technical report, University of Waterloo, May 1994.

[155] B. M. Riess, February 1995. Personal communication.

[156] B. M. Riess, K. Doll, and F. M. Johannes. Partitioning very large circuits using analytical placement techniques. In *Proc. ACM/IEEE Design Automation Conf.*, pages 646–651, 1994.

[157] B. M. Riess, H. A. Giselbrecht, and B. Wurth. A new k-way partitioning approach for multiple types of fpgas. Technical Report TUM-LRE-95-2, Technical University of Munich, 1995.

[158] B. M. Riess and A. A. Schoene. Architecture driven k-way partitioning for multichip modules. In *Proc. European Design and Test Conf. (to appear)*, 1995.

[159] K. Roy and C. Sechen. A timing-driven n-way chip and multi-chip partitioner. In *Proc. IEEE Intl. Conf. Computer-Aided Design*, pages 240–247, 1993.

[160] Y. Saab. A fast and robust network bisection algorithm. *IEEE Trans. Computers (to appear)*, 1995.

[161] Y. Saab. New methods for construction of test cases for partitioning heuristics. *Progress in VLSI Design (to appear)*, 1996.

[162] Y. Saab and V. Rao. Fast effective heuristics for the graph bisectioning problem. *IEEE Trans. Computer-Aided Design*, 9(1):91–98, January 1990.

[163] Y. Saab and V. Rao. On the graph bisection problem. *IEEE Trans. Circuits and Systems*, 39(9):760–762, September 1992.

[164] L. A. Sanchis. Multiple-way network partitioning. *IEEE Trans. Computers*, 38(1):62–81, January 1989.

[165] L. A. Sanchis. Multiple-way network partitioning with different cost functions. *IEEE Trans. Computers*, 42(22):1500–1504, 1993.

[166] H. Saran and V. V. Vazirani. Finding k-cuts within twice the optimal. In *Proc. IEEE Symp. Foundations of Computer Science*, pages 743–751, 1991.

[167] G. Saucier, D. Brasen, and J. P. Hiol. Partitioning with cone structures. In *Proc. IEEE Intl. Conf. Computer-Aided Design*, pages 236–239, 1993.

[168] D. M. Schuler and E. G. Ulrich. Clustering and linear placement. In *Proc. ACM/IEEE Design Automation Conf.*, pages 50–56, 1972.

[169] D. G. Schweikert and B. W. Kernighan. A proper model for the partitioning of electrical circuits. In *Proc. ACM/IEEE Design Automation Conf.*, pages 57–62, 1972.

[170] C. Sechen and D. Chen. An improved objective function for mincut circuit partitioning. In *Proc. IEEE Intl. Conf. Computer-Aided Design*, pages 502–505, 1988.

[171] N. A. Sherwani. *Algorithms for VLSI Physical Design Automation.* Kluwer Academic Publishers, Boston, 1993.

[172] M. Shih, 1993. Personal communication.

[173] M. Shih and E. Kuh. Quadratic boolean programming for performance-driven system partitioning. In *Proc. ACM/IEEE Design Automation Conf.*, pages 761–765, 1993.

[174] M. Shih, E. Kuh, and R.-S. Tsay. Performance-driven system partitioning on multi-chip modules. In *Proc. ACM/IEEE Design Automation Conf.*, pages 53–56, 1992.

[175] M. Shih, E. Kuh, and R.-S. Tsay. Timing-driven system partitioning by constraints decoupling method. In *Proc. IEEE Multi-Chip Module Conf.*, pages 164–169, 1993.

[176] H. Shin and C. Kim. A simple yet effective technique for partitioning. *IEEE Trans. VLSI Systems*, 1(3), September 1993.

[177] G. Sigl, K. Doll, and F. M. Johannes. Analytical placement: A linear or a quadratic objective function? In *Proc. ACM/IEEE Design Automation Conf.*, pages 427–432, June 1991.

[178] P. R. Suaris and G. Kedem. An algorithm for quadrisection and its application to standard cell placement. *IEEE Trans. Circuits and Systems*, 35(3):294–303, 1988.

[179] W. Sun and C. Sechen. Efficient and effective placements for very large circuits. In *Proc. IEEE Intl. Conf. Computer-Aided Design*, pages 170–177, 1993.

[180] L. Tao, Y. C. Zhao, K. Thulasiraman, and M. N. S. Swamy. An efficient tabu search algorithm for graph bisectioning. In *Proc. Great Lakes Symp. VLSI*, pages 92–95, 1991.

[181] M. Toyonaga, S.-T. Yang, T. Akino, and I. Shirakawa. A new approach of fractal-dimension based module clustering for vlsi layout. In *Proc. IEEE Intl. Symp. Circuits and Systems*, pages 185–188, 1994.

[182] S. Tragoudas. An improved algorithm for the generalized min-cut partitioning problem. In *Proc. Great Lakes Symp. VLSI*, pages 242–247, 1994.

[183] R.-S. Tsay and E. S. Kuh. A unified approach to partitioning and placement. *IEEE Trans. Circuits and Systems*, 38(5):521–533, 1991.

[184] A. Vannelli and S. W. Hadley. A gomory-hu cut tree representation of a netlist partitioning problem. *IEEE Trans. Circuits and Systems*, 37(9):1133–1139, 1990.

[185] A. Vannelli and G. S. Rowan. A constrained clustering approach for partitioning netlists. In *Proc. 28th Midwest Symposium on Circuits and Systems*, pages 211–215, 1985.

[186] G. Vijayan. Generalization of min-cut partitioning to tree structures and its applications. *IEEE Trans. Computers*, 40(3):307–314, 1991.

[187] Y.-C. Wei and C.-K. Cheng. Towards efficient hierarchical designs by ratio cut partitioning. In *Proc. IEEE Intl. Conf. Computer-Aided Design*, pages 298–301, 1989.

[188] Y.-C. A. Wei and C.-K. Cheng. An improved two-way partitioning algorithm with stable performance. *IEEE Trans. Computer-Aided Design*, 10(12):1502–1511, 1991.

[189] N.-S. Woo and J. Kim. An efficient method of partitioning circuits for multiple-fpga implementation. In *Proc. ACM/IEEE Design Automation Conf.*, pages 202–207, 1993.

[190] H. Yang and D. F. Wong. Efficient network flow based min-cut balanced partitioning. In *Proc. IEEE Intl. Conf. Computer-Aided Design*, pages 50–55, 1994.

[191] H. Yang and D. F. Wong. Circuit clustering for delay minimization under area and pin constraints. In *Proc. European Design and Test Conf. (to appear)*, 1995.

[192] H. Yang and D. F. Wong. Optimal wiring minimization for partitioned circuits with least replication. Manuscript, 1995.

[193] C.-W. Yeh, C.-K. Cheng, and T.-T. Y. Lin. A probabilistic multi-commodity flow solution to circuit clustering problems. In *Proc. IEEE Intl. Conf. Computer-Aided Design*, pages 428–431, 1992. Also see *IEEE Trans. on CAD*, **14**:(2), pp. 154-162, 1995, for extended version.

[194] C.-W. Yeh, C.-K. Cheng, and T.-T. Y. Lin. A general purpose, multiple-way partitioning algorithm. *IEEE Trans. Computer-Aided Design*, 13(12):1480–1487, 1994.

[195] C.-W. Yeh, C.-K. Cheng, and T.-T. Y. Lin. Optimization by iterative improvement: An experimental evaluation on two-way partitioning. *IEEE Trans. Computer-Aided Design*, 14(2):145–153, February 1995.

[196] H. J. Zimmerman. *Fuzzy Set Theory and its Applications.* Kluwer Nlijhoff, 2nd edition, 1991.