CAD-IP Reuse via the Bookshelf for Fundamental VLSI CAD Algorithms

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Outline

- Sample problems in EDA industry
  - lack of qualified VLSI CAD engineers
  - time-to-market
  - often, no feel for QOR
- Sample problems in academic research
  - focus on isolated optimizations; no good evaluation of QOR
  - potentially outdated understanding of design processes
- IP-based solution, a culture change
  - Notion of CAD-IP (reuse), incentives for developing CAD-IP and reusing it
  - Need infrastructure for developing, cataloguing and distributing CAD-IP
- CAD-IP reuse via the MARCO/GSRC Bookshelf; current status
- Futures
Sample Problems in EDA industry

◆ Lack ("insufficient supply") of qualified VLSI CAD engineers
  ▲ 100s of companies may re-implement same algorithms
    ▼ wasted resources compound the problem of insufficient supply

◆ Time to market (5-7 year delay from publishing to first industrial use)
  ▲ academic papers often lack empirics ⇒ every user re-runs empirics
  ▲ tool integration (academics tend to focus on isolated optimizations)
  ▲ changes in technology and design processes

◆ Quality of result (QOR)
  ▲ often cannot be evaluated in an isolated [optimization] context
  ▲ CAD engineers have no feel for QOR

Sample Problems in Academic Research

◆ Focus on narrow optimizations
  ⇒ sometimes no ability to evaluate QOR (in a relevant way)
  ⇒ no feel for QOR
  ⇒ impact of research severely limited

◆ Potentially outdated understanding of design processes
  ▲ Example in placement: fixed-die reality vs. variable-die research
    (see paper 27.5 in DAC Proceedings)

◆ “Lack of communication”
  ▲ lack of communication with industry (see above)
  ▲ lack of communication with each other
    (a 1999 paper on partitioning ignored all partitioning literature of 1994-99)
  ▲ even “all-to-all communication” (everyone reads every paper) will fail
  ▲ solution: more efficient evaluation, comparison and filtering
Solution by reuse

- What is to be re-used: “CAD-IP”
  - Data models and benchmarks
    - context descriptions and use models
    - testcases and good solutions
  - Algorithms and algorithm analyses
    - mathematical formulations
    - comparison and evaluation methodologies for algorithms
    - executables and source code of implementations
    - leading-edge performance results
  - Traditional (paper-based) publications (6-page 2-column papers)

- Encourage reuse by crediting it: culture change

- Create and maintain infrastructure for reuse
  - related: open-source culture

The GSRC Bookshelf for CAD-IP

- Bookshelf consists of slots
  - slots represent active research areas with “enough customers”
  - collectively, the slots cover the field

- Who maintains slots?
  - experts in each topic collaborate to produce them - anyone can contribute

- Currently, over 15 active slots
  - SAT (U. Michigan, Sakallah)
  - Graph Coloring (UCLA, Potkonjak)
  - Hypergraph Partitioning (UCLA, Kahng)
  - Block Packing (UCSC, Dai)
  - Placement (UCLA, Kahng)
  - Global Routing (SUNY Binghamton, Madden)
  - Single Interconnect Tree Synthesis (UIC, Lillis and UCLA, Cong)
  - Recent additions: Mathematical programming, BDDs, Clock Routing trees etc.
What’s in a Slot?

◆ Introduction
  ▲ why this area is important and recent progress
  ▲ pointers to other resources (links, publications)
◆ Data formats used for benchmarks
  ▲ SAT, graph formats etc.
  ▲ new XML-based formats
◆ Benchmarks, solutions, performance results
  ▲ including experimental methodology (e.g., runtime-quality Pareto curve)
◆ Binary utilities
  ▲ format converters, instance generators, solution evaluators, legality checkers
  ▲ optimizers and solvers
  ▲ executables
◆ Implementation source code
◆ Other info relevant to algorithm research and implementations
  ▲ detailed algorithm descriptions
  ▲ algorithm comparisons

UCLA PD Tools release (June 2, 2000)

◆ 118K lines in C++ under MIT open-source license
  http://vlsicad.cs.ucla.edu/software/PDtools
  Also: openeda.org  edacafe.com  ASPs (toolwire.com) ...
◆ 34 packages connected using shared libraries, ~3MB total
  ▲ Capo placer, MLPart partitioner, UCLA DB, parsers, support libs
◆ Installation script for Unix systems (Solaris, Linux etc.)
◆ No package version management (but the distribution itself is versioned)
◆ MSVC++ configuration: more work needed
Contributing to Bookshelf

- Request membership in the bookshelf group at http://www.gigascale.org
  - ask for "developer" membership (as applicable)
  - go over existing slots related to your research
  - browse mail archives
- Are you creating a new bookshelf slot?
  - Yes (no existing slots are appropriate)
    - use slot template from Web page (fill in the blanks)
    - write intro
    - give references to relevant sites
    - mail the URL (or the HTML) to bookshelf developers
  - No (contribution to an existing slot)
    - agree with the maintainers of the slot about your contribution
      - e.g., convert LaTeX tables from conference papers into HTML by tth
    - mail URL or your contributions to slot maintainers

Future Directions: New Tool Flows

- Recent splash of interest to placement among researchers
  - At least 6-7 academic groups have working placers
  - At least 3 placers support Bookshelf file format
- Always need to evaluate results with a router
- UCLA/ABK group assembled such a flow for plug-in placer
- Using Bookshelf formats (and converters to/from LEF/DEF)
  - can now test other academic placers with commercial routers
  - can mix and match constructive and iteratively improving placers
  - can mix and match global and detailed placers
Conclusions

- The Bookshelf is accepting contributions
- The Bookshelf gets a lot of hits
- The Bookshelf helps doing research
  - has clear problems formulations
  - offers a catalogue of available implementations
  - facilitates comparisons and evaluations that may be hard OW
- The Bookshelf reduces waste by improving reuse
- The Bookshelf helps the EDA industry
  - Points out academic research “that actually works”
  - Gives access to more open-source codes

http://vlsicad.cs.ucla.edu/GSRC/bookshelf/