

**SITS**

**Single Interconnect Tree Synthesis  
slot status**

John Lillis

Miloš Hrkić

University of Illinois at Chicago

# Status

- Rev 1.2 of file formats
- Two solvers posted + TRIO
  - P-Tree (Linux & Solaris executable)
  - S-Tree (Linux & Solaris executable)
- GUI versions in progress (demo)
- Sample instances available

# To Do List

- Synchronize data formats with Fundamental Technology slot (Oct 15)
- Post two more solvers
  - Static topology optimizer (Oct 20)
  - Soft edges topology optimizer (Oct 25)
- GUI versions of all 4 solvers (Nov 10)
- Industrial benchmark instances?
- Post source codes (Nov 15)