Hurwitz Interconnect Delay Evaluation - HIDE

User's Manual

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1. Introduction

The purpose of HIDE is to evaluate delays of an RLC interconnect tree very accurately and scale the original tree structure down to a set of equivalent, connected, and realizable π models.

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The program features:

- Delay evaluation with user-defined threshold;
- Rise time evaluation with user-defined starting and end thresholds;
- Waveform evaluation for user-defined test node(s);
- Equivalent load generation for gate delay evaluation;
- Hspice-formatted netlist generation for delay result verification;
- Moment generation for each node.

These features and their useage will be introduced in detail in sec. 4.

2. Supported Input Signals

Three input signals are supported in the program: exponential, ramp, and step functions. Users can specify the input signal type and the corresponding control parameters in an *input command file* (see sec. 4).

- Exponential function:

$$V(t) = \left(1 - e^{-\frac{t}{tr}}\right)U(t) \qquad t \geq 0 \qquad (1)$$

- Ramp function:

$$V(t) = \begin{cases} \frac{t}{tr} & 0 \leq t \leq tr \\ 1 & t > tr \end{cases} \qquad (2)$$

- Step function:

$$V(t) = 1 \qquad t \geq 0 \qquad (3)$$

where tr is the rise time of the input signal, which is defined in an input command file (see sec. 4), and $U(t)$ is the unit step function.

3. Supported Delay Evaluation

For delay evaluation, presently we provide three delay models:

- Elmore delay model;
- D2M delay model;
- HIDE delay model.

The first two are provided for comparisons with our HIDE model. So features such as waveform evaluation, delay metrics for user-defined threshold(0% ~ 100% of V_{DD}), and rise time for user-

defined starting and ending delay threshold (0% ~ 100% of V_{DD}) are provided only for HIDE delay model. As for Elmore delay model and D2M delay model, we only provide general delay metrics.

4. Format of Input Command File

*keyword are highlighted.

InputFile: *< input file name >*

InputFile specifies a spice or dspf formatted input netlist file. Note that HIDE as Interconnect Delay Evaluation package, can only handle tree structured RLC circuits.

OutputFile: *< output file name >*

OutputFile specifies the output file in which all the evaluation results are going to be saved.

InputFileFormat[dspf/spice]: *< dspf | spice >*

InputFileFormat defines the input netlist file format. This file is the one specified in **InputFile** entry.

IsGenHspiceNetlist[Yes/No]: *< Yes | No >*

IsGenHspiceNetlist tells HIDE if the input netlist file needs to be translated into an Hspice-formatted file. This entry should be checked as <*yes*> and the next entry **Fspice** should also be specified if you want to compare HIDE with Hspice.

Fspice: *<hspice-formatted input netlist file name>*

Fspice specifies the hspice-formatted input netlist file name. This file is translated from the file indicated in **InputFile** entry. **Fspice** should be checked correctly if **IsGenHspiceNetlist** is checked as <*yes*>. But **Fspice** will be ignored if **IsGenHspiceNetlist** is checked as <*No*>.

InputSignalType[exp/ramp/step]: *< exp | ramp | step >*

InputSignalType defines the input signal type. <*exp*> denotes the input signal as an exponential function, <*ramp*> as a ramp function, and <*step*> as a step function. Presently only these three types are supported.

InputSignalRiseTime: $<tr>$

InputSignalRiseTime is the parameter defined in equation (1) and (2) above.

DelayThreshold[0-1.0]: $<Delay_{th}>$

DelayThreshold defines the delay observation point at which the output signal is $(Delay_{th} \times 100)$ percentage of V_{DD}. It is effective to HIDE delay model only.

IsRiseTime[Yes/No]: *< Yes | No >*

IsRiseTime tells HIDE if the rise time of the output signal needs to be printed out. It is effective to HIDE delay model only.

RiseTimeStart[0-0.5]: $< Delay_{start} >$

RiseTimeStart defines the starting delay observation point at which the output signal is $(Delay_{start} \times 100)$ percentage of V_{DD}. It is used with **RiseTimeEnd** together. And it is effective to HIDE delay model only.

RiseTimeEnd[0.5-1.0]: $< Delay_{end} >$

RiseTimeEnd defines the end delay observation point at which the output signal is $(Delay_{end} \times 100)$ percentage of V_{DD}. It is used with **RiseTimeStart** together to specify the output voltage range that users are interested in. It is effective to HIDE delay model only.

IsOutputWaveform[Yes/No]: *< Yes | No >*

IsOutputWaveform tells HIDE if the output waveform needs to be printed out. This entry is optional. It is effective to HIDE delay model only.

BeginWaveFormParameters
Vdd *< power supply voltage >*
tstep *< step size >* /
tstop *< stop time >*

EndWaveFormParameters

This option is optional and will be ignored if **IsOutputWaveform** is checked as <*No*>. The starting time is assumed to be zero.

IsGenMoment[Yes/No]: < *Yes* | *No* >

IsGenMoment is optional and if it is checked as <*Yes*>, HIDE will calculate the moments up to the third order and print them out.

IsElmore[Yes/No]: < *Yes* | *No* >

IsElmore is optional and if it is checked as <*Yes*>, HIDE will calculate Elmore delay and print it out. Note that presently, Elmore delay is calculated without considering input signal, i.e., it is independent from input signal

IsD2M[Yes/No]: < *Yes* | *No* >

IsD2M is optional and if it is checked as < *Yes* >, the program will calculate D2M delay metrics and print it out. Note that presently, D2M delay is calculated without considering input signal, i.e., it is independent from input signal

IsDebug[Yes/No]: < *Yes* | *No* >

IsDebug is optional and only useful for programmers. When it is checked as < *Yes* >, more detailed runtime information will be printed out.

IsOutputAll[Yes/No]: < *Yes* | *No* >

IsOutputAll is optional and if it is checked as < *Yes* >, all the nodes in the input netlist file will be printed out.

IsUseDefaultTestNode[Yes/No]: < *Yes* | *No* >

IsUseDefaultTestNode is optional and if it is checked as < *Yes* >, **TestNodeList** entry will be read in and HIDE will only print out delays for listed test nodes.

TestNodeList:
<Node Name ... ... >
EndTestNodeList

This entry specifies the test nodes that users are interested in. If a test node defined by user is not found in the netlist, this node will be ignored and a warming message may be printed out. See **IsUseDefaultTestNode** for details.

Bug report

Please feel free to contact Zhanhai Qin via zqin@cs.ucsd.edu or 1-858-534-8174 if you found any bugs in the program or if you have any idea to help us improve it.